

5 a plurality of contacts including a first plurality of contacts and a second
6 plurality of contacts, said first plurality of contacts located in the second region, and
7 said second plurality of contacts located in the first region such that a smallest
8 distance between adjacent contacts in the first region is different than a distance
9 between the first and second regions, wherein the third region does not have any
10 contacts located therein.

1 ²~~18~~ The semiconductor package of claim ¹~~17~~, wherein the smallest distance
2 between adjacent contacts in the first region is smaller than the distance between the
3 first and second regions.

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1 ³~~19~~ The semiconductor package of claim ¹~~17~~, wherein the smallest distance
2 between adjacent contacts in the first region is larger than the distance between the
3 first and second regions.

1 ⁴~~20~~ The semiconductor package of claim ¹~~17~~, wherein the semiconductor
2 package is a ball grid array package.

1 ⁵~~21~~ The semiconductor package of claim ¹~~17~~, wherein the plurality of
2 contacts comprises a plurality of contact pads.

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1 ⁶~~22~~. The semiconductor package of claim ⁵~~21~~ further comprising a plurality
2 of solder balls attached to said contact pads.

1 ⁷~~23~~. The semiconductor package of claim ¹~~17~~ wherein each of the second
2 plurality of contacts is contained within a dimensional profile of an integrated
3 circuit coupled to the top surface of the substrate.

1 ⁸~~24~~. The semiconductor package of claim ¹~~17~~ wherein the plurality of
2 contacts are located on the exposed external opposite surface of the substrate.

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1 ⁹~~25~~. The semiconductor package of claim ¹~~17~~ wherein said top surface of
2 said substrate has a plurality of bond pads.

1 ¹⁰~~26~~. The semiconductor package of claim ⁹~~25~~ wherein said top surface of
2 said substrate has a ground bus that is connected to said second plurality of contacts
3 by a plurality of vias that extend through said substrate.

1 ¹¹~~27~~. The semiconductor package of claim ¹~~17~~ wherein said first plurality of
2 contacts comprises at least five rows of contacts.

1 ¹²~~28~~ The semiconductor package of claim ⁹~~25~~ wherein said top surface of
2 said substrate has a power bus that is connected to said second plurality of contacts
3 by a plurality of vias that extend through said substrate.

1 ¹³~~29~~ The semiconductor package of claim ¹~~17~~, wherein said second plurality
2 of contacts is arranged in a four by four matrix.

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1 ¹⁴~~30~~ A semiconductor package, comprising:
2 a substrate that includes a top surface having a plurality of bond pads, and an
3 exposed external opposite surface defined by an inner region, an outer region, and a
4 middle region that separates the inner and outer regions;
5 a plurality of contacts including a first plurality of contacts and a second
6 plurality of contacts, said first plurality of contacts located in the outer region, and
7 said second plurality of contacts located in the inner region such that a first smallest
8 distance between adjacent contacts in the inner region is different than a second
9 smallest distance between the inner and outer regions, wherein the middle region is
10 free of contacts; and
11 an integrated circuit that is mounted to said top surface of said substrate and
12 coupled to said plurality of bond pads.

1 ¹⁵~~31~~ The semiconductor package of claim ¹⁴~~20~~, wherein the first smallest
2 distance is smaller than the second smallest distance.

1 ¹⁶~~32~~. The semiconductor package of claim ¹⁴~~30~~, wherein the first smallest
2 distance is larger than the second smallest distance.

1 ¹⁷~~33~~. The semiconductor package of claim ¹⁴~~30~~, wherein the semiconductor
2 package is a ball grid array package.

1 ¹⁸~~34~~. The semiconductor package of claim ¹⁴~~30~~ further comprising a plurality
2 of solder balls attached to said plurality of contacts.

a1 1 ¹⁹~~35~~. The semiconductor package of claim ¹⁴~~30~~ wherein said top surface of
2 said substrate has a ground bus that is coupled to said integrated circuit and
3 connected to said second plurality of contacts by a plurality of vias that extend
4 through said substrate.

1 ²⁰~~36~~. The semiconductor package of claim ¹⁴~~30~~ wherein said top surface of
2 said substrate has a power bus that is coupled to said integrated circuit and
3 connected to said second plurality of contacts by a plurality of vias that extend
4 through said substrate.

1 ²¹~~37~~. The semiconductor package of claim ¹⁴~~30~~ wherein said integrated circuit
2 is enclosed by an encapsulant.

1 ²²~~38~~. The semiconductor package of claim ¹⁴~~30~~ wherein said first plurality of
2 contacts is located outside an outer dimensional profile of said integrated circuit.

1 ²³~~39~~. The semiconductor package of claim ²²~~38~~ wherein said second plurality
2 of contacts is located inside the outer dimensional profile of said integrated circuit.

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1 ²⁴~~40~~. An integrated circuit package for an integrated circuit which has a
2 dimensional profile, comprising:
3 a substrate that includes a top surface, and an exposed external opposite
4 surface defined by a first region that is substantially equal to the dimensional profile
5 of the integrated circuit, a second region, and a third region that separates the first
6 and second regions; and
7 a plurality of contacts including a first plurality of contacts and a second
8 plurality of contacts, said first plurality of contacts located within the second region,
9 and said second plurality of contacts located in the first region such that a first
10 smallest distance between adjacent contacts in the first region is smaller than a
11 second smallest distance between the first and second regions, said third region
12 being a contact free region.

1 ²⁵~~41~~. The integrated circuit package of claim ²⁴~~40~~, wherein a distance between
2 adjacent contacts in first region is the same as the distance between adjacent contacts
3 in the second region.

1 ²⁶~~42~~ The integrated circuit package of claim ²⁴~~40~~ further comprising a
2 plurality of solder balls attached to said plurality of contacts.

1 ²⁷~~43~~ The integrated circuit package of claim ²⁴~~40~~ wherein said top surface of
2 said substrate has a ground bus that is connected to said second plurality of contacts
3 by a plurality of vias that extend through said substrate.

1 ²⁸~~44~~ The integrated circuit package of claim ²⁴~~40~~ wherein said top surface of
2 said substrate has a power bus that is connected to said second plurality of contacts
3 by a plurality of vias that extend through said substrate.


REMARKS

Applicant submits this Preliminary Amendment canceling claims 1-16 and adding claims 17-44. Examination of the pending claims at the Examiner's earliest convenience is respectfully solicited.

Respectfully submitted,

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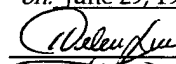


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Helen Zuc

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